LVPECL, PECL, ECL Logic and Termination

ABSTRACT

This application note will highlight characteristics of Pletronics Low Voltage Positive Emitter Coupled Logic (LVPEC quency control products and provide guidance for proper termination.

This logic type is significantly different than TTL or CMOS logic and does require special consideration to utilize the properly. For example, without any termination the ECL/PECL will not work.

The terms ECL, PECL and LVPECL are reviewed.

- PECL to CML
- PECL to LVDS
- PECL to PECL
- PECL to HSTL

The logic is important in that:

- It provides very high frequency operation.
- Typically, the clock signals are differential which minimizes EMIRFI.
- Output terminations are low impedance and permit practical implementation on the final system requirements.

The application of the Pletronics PE7, PE9 LVPECL families is reviewed. The Pletronics VPU7 VCXO family is a similar design to the PE9 series; therefore, all of the following examples also apply to the VPU7 series.

In this document, PECL and LVPECL are used interchangeably. The LV was added to indicate low voltage when the 5.0V devices were lowered to 3.3V. Today, we have 5.0V, 3.3V, 2.5V and just the beginning of 1.8V devices, hence the LV has lost most of its meaning.

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LVPECL, PECL, ECL Logic and Termination

TABLE OF CONTENTS

LVPECL, PECL, ECL Logic and Termination

1 INTRODUCTION

This section is for those who are not familiar with ECL-PECL devices. This logic family has many different characteristics than any of the other logic families. It is fast and permits some of highest speeds of operation.

1.1 HISTORY OF ECL

ECL was first introduced in IC form in 1962 by Motorola as their monolithic emitter coupled logic (MECL 1). It is one of the oldest forms of IC logic. This form of logic resulted in faster operating speeds than DTL or TTL and also integrated well into the IC process:

It is dependent on resistor ratios, not absolute values
The transistors all being matched made the design easier.
The transistors operate in the linear region or off, never in the saturated mode which adds processing steps to allow the transistors to quickly recover.
Many of the components fit into one isolated region which results in efficient die size.

The power dissipation is very high compared to other solutions. The outputs of all devices are designed to be terminated and the signal swings are small. These points give ECL unique characteristics.

This ECL logic has continued to evolve and is now usable in the GHz range. This has followed the ever shrinking semiconductor device sizes and is implemented with RF SiGe processes for low noise and best speed.

LVDS and PECL output levels

Output	LVDS	PECL 3.3V	PECL 2.5V
V_{OH} (Minimum)	1.249 V	2.27 V	1.47 V
V_{OL} (Maximum)	1.252 V	1.68 V	0.88 V

The LVDS levels do not change with supply voltage.

The PECL output levels follow the supply voltage. The values shown are for the nominal supply voltage only.

LVDS and PECL input levels

Input	LVDS	PECL 3.3V	PECL 2.5V	HSTL	CML
V_{REF} or V_{CM}	1.20 V	2.00 V	1.20 V	0.75 V	V_{CC} - 0.20 V
V_{ID} (Minimum)	200 mV	310 mV	310 mV	400 mV	400 mV
V_{IH} (Minimum)	1.249 V	2.27 V	1.47 V	V_{REF} + 0.2 V	V_{CC}
V_{IL} (Maximum)	1.252 V	1.68 V	0.88 V	V_{REF} - 0.2 V	V_{CC} - 0.40 V

LVPECL, PECL, ECL Logic and Termination

1.2 How ECL Logic Works

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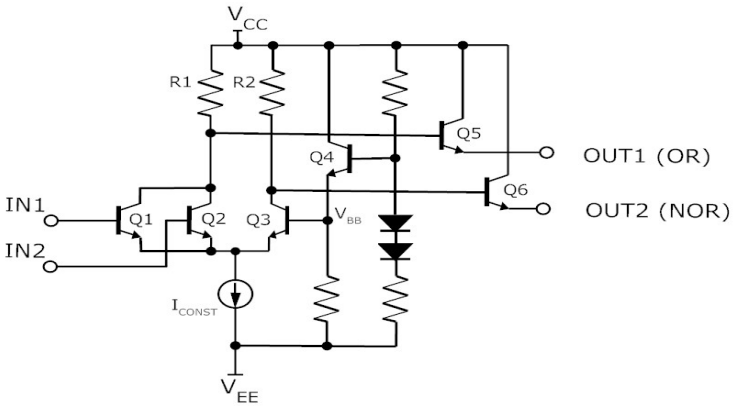


The basic gate is shown below:

If both IN1 and IN2 are below V_{BB} then:

- all of the current of I_{CONST} will pass through Q3. In fact IN1 and IN2 only needs to be about 120mV below V_{BB} for current in R2 to be 100 times that in R1.
- the voltage drop across R1 is only the base current of Q5. The logic high (V_{HI}) then is about one V_{BE} (1 diode drop) below the positive supply.
- the goal of being able to connect to more logic gates and not have a transistor in saturation (collector voltage much below the base voltage), the logic level or swing needs to be about one V_{BE}. Therefore, the logic low (V_{LO}) is about two V_{BE} amounts.

If either or both IN1 and IN2 are above V_{BB} then:

- all of the current of I_{CONST} will pass through Q1 or Q2. In fact IN1 and IN2 only need to be about 120mV above V_{BB} for current in R1 to be 100 times that in R2.
- the voltage drop across R2 is only the base current of Q6. The logic high (V_{HI}) is then about one V_{BE} (1 diode drop) below the positive supply.
- the drop across R1 will be about one V_{BE} and therefore OUT2 will be about two V_{BE} drops below the positive supply.

The ECL type output is an emitter of a transistor. There is no pull down, and therefore the pull down has to be external. This is done for several reasons:

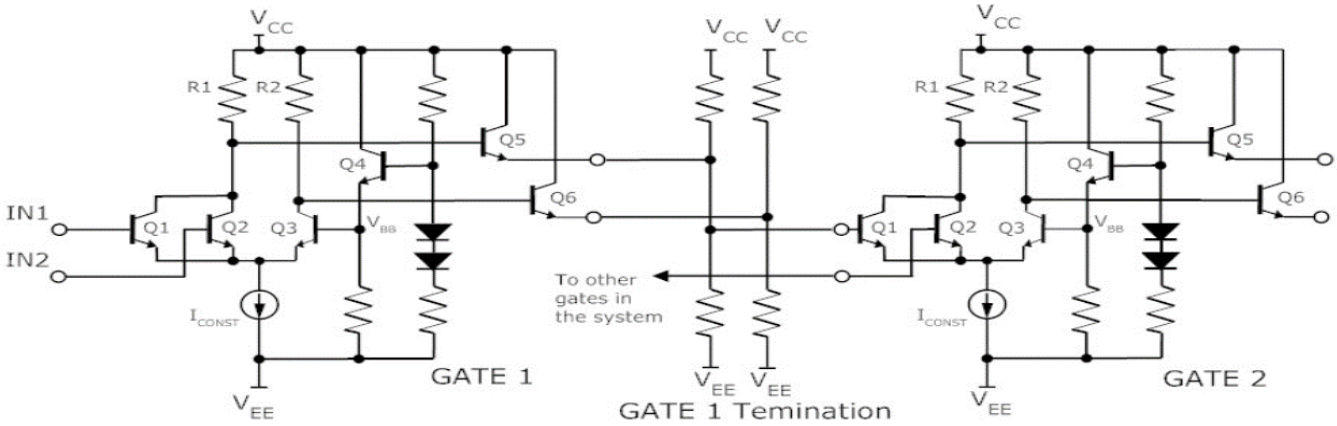
- This logic is intended very high speeds, therefore the lines need to be terminated to control ringing and reflections from the transmission line ends. Emitter followers provide a low impedance output to work with terminations.
- Terminations are normally in the 25 ohm to 100 ohm range. This would result in excessive power in the IC if done internally to ground.

LVPECL, PECL, ECL Logic and Termination

- The termination is normally done as 50 ohms to a node that is 2.0 volts below the positive supply node.
- The outputs can be tied together when doing logic gates. This forms another logic point called “wired-OR” that does not add any added gate delays.

1.3 How ECL Connects in a System

The above logic gate can be connected to other gates to begin to perform a system function.



It is important that both outputs are terminated for best performance. If only one output is used, the duty cycle and jitter can be adversely affected.

In this example the GATE 1 output is terminated and one signal then connects to GATE 2 where the other GATE 2 input can come from some other ECL signal in the system.

Since the logic levels are referenced to the positive lead and the logic levels are small, the positive power supply distribution is critical for best noise immunity and jitter performance.

1.4 What differentiates ECL, PECL and LVPECL?

There is no difference between ECL, PECL or LVPECL.

For this type of circuit, the current in the negative lead is nearly a constant with no switching transients. The differential stage is biased with a constant current source. The V_{BB} derivation leg is resistive and does not change with input level.

The positive power lead has the transients of the output charging any mismatched capacitive loads.

LVPECL, PECL, ECL Logic and Termination

ECL was chosen to operate from ground to a negative supply. Therefore the device leads with the most transients is connected into the ground plane. This resulted in the logic levels which are referenced to ground and became somewhat independent of power supply voltage.

With so many systems operating with TTL or CMOS logic at 5.0V, designers began using ECL with the positive lead connected to +5.0V and the negative lead grounded. This increased some design and layout needs but it also meant there was one less power supply need in the system. So if ECL is operated positive, the ECL is Positive ECL or PECL. It is important to note, this is a nomenclature change but the IC involved needed no changes.

In time the system power supply voltages were lowered, typically to 3.3V and 2.5V and the term Low Voltage Positive Emitter Coupled Logic (LVPECL) was coined.

Summary, the schematic of ECL, PECL and LVPECL can be the same, the resistor values may change for the lower voltages. These terms are more marketing based than changes in technology.

1.5 What differentiates the Pletronics PE7and PE9 series clock oscillators?

Pletronics provides an assortment of PECL output solutions. These solutions all meet the typically accepted PECL specification. These differ in the method of achieving the output frequency.

Characteristics	PE7	PE9
Crystal Mode Used	3rd Overtone	Fundamental
Frequency Range	80 to 325MHz	10.9MHz to 1.1GHz
Supply Voltage	2.5V and 3.3V	3.3V
Multiplication Method	none	Low Noise PLL with an LC VCO phase locked to the crystal
Process Technology	BiCMOS	RF SiGe BiCMOS
Phase Noise	In close phase noise excellent	---
Jitter	Excellent	Good
Tr and Tf	Good	Excellent (very fast)

The Pletronics PECL VCXO series is derived from the PE9 device and therefore has the same characteristics as the PE9 series.

LVPECL, PECL, ECL Logic and Termination

2 Terminations for the PE7 and PE9 Series Clock Oscillators

This application note will highlight characteristics of Pletronics Low Voltage Positive Emitter Coupled Logic (LVPECL) frequency control products and provide guidance for proper termination.

Unlike many logic families, ECL, PECL and LVPECL are not standardized. ECL and its derivatives originated from a vendor's implementation of ECL. The original embodiment of ECL established V_{CC} at ground potential and V_{EE} at -5.2 volts. PECL is functionally the same as ECL but uses a positive rather than negative power supply voltage by connecting V_{CC} to the positive supply and V_{EE} to ground. LVPECL is merely PECL designed for use with power supply voltages lower than 5v. Typical voltages are 3.3v, 2.5v and 1.8v. The following table provides typical output signal levels for Pletronics LVPECL frequency control devices.

Family		PE7	PE7	PE9
V_{CC}		2.5V	3.3V	3.3V
Output High Logic Level (V_{HI})	Referenced to V_{CC}	-1.025V	-1.125V	-1.180V
	Referenced to Ground	1.475V	2.275V	2.120V
	Referenced to V_{TT}	0.975V	0.975V	1.190V
Output Low Logic Level (V_{LO})	Referenced to V_{CC}	-1.405V	-1.620V	-1.310V
	Referenced to Ground	1.095V	1.680V	1.990V
	Referenced to V_{TT}	0.595V	0.380V	0.690V

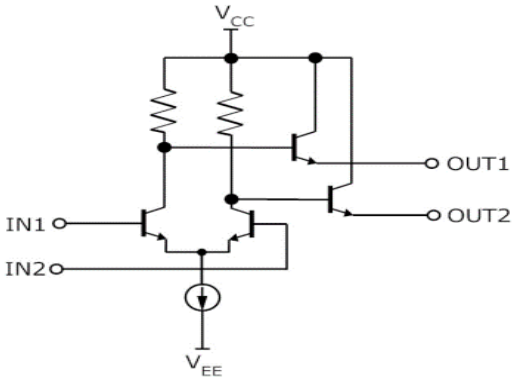
As system speeds have increased, the low peak-to-peak voltage and differential nature of PECL have proven to be very attractive to system architects. LVPECL is now widely accepted as a mainstay of many high speed, controlled impedance, I/O structures.

Traditionally ECL, in its multitude of forms, uses a differential bi-polar input stage and differential emitter follower output stage. In order to reduce power consumption, the output stage does not include an internal pull-down resistor. The emitter follower output stage relies on the external termination network to perform the pull down. This is a simplified schematic of an ECL line receiver gate.

of their circuit structures have been used. These implementations, which may be in bi-polar, CMOS, etc., can include internal active totem pole or passive pull-down output structures. These structures provide a current return path so an output signal will be observed without a termination network.

LVPECL, PECL, ECL Logic and Termination

The output structure of Pletronics LVPECL frequency control devices is a bi-polar, differential, emitter follower stage without internal pull-down resistors. Therefore, a termination network is necessary for proper output signals to be observed.



It must also be noted that the LVPECL differential input requires a common mode reference voltage. This voltage is nominally Vcc – 2.0V. For 3.3v LVPECL, this common mode reference supply is 1.3v. Extra power supplies are not attractive so alternative termination schemes will be shown.

We receive questions from time to time regarding why one vendor's PECL device functions without pull-down termination resistors and another vendor's part does not. As mentioned earlier, ECL and its various derivatives are not standardized. So in addition to ECL, PECL and LVPECL derivatives, numerous implementations of their circuit structures have been used. These implementations, which may be in bi-polar, CMOS, etc., can include internal active totem pole or passive pull-down output structures. These structures provide a current return path so an output signal will be observed without a termination network.

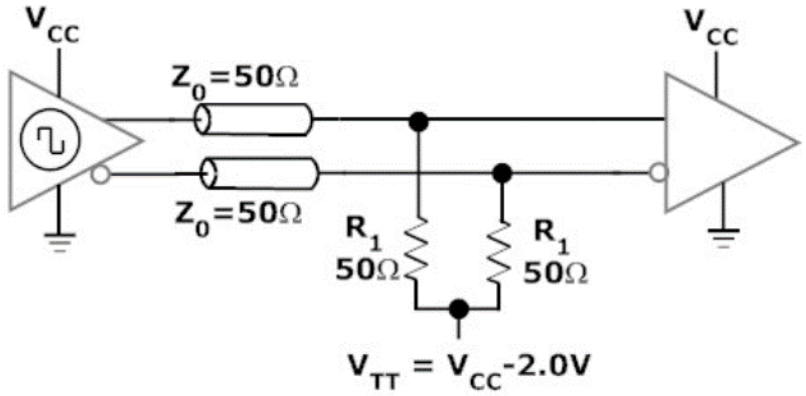
2.1 PECL Termination

There are a multitude of termination schemes used for LVPECL which fall into two broad classes – DC coupled and AC coupled. Within these two classes, there are other possibilities, depending on the particular circuit requirements. When selecting an oscillator, the voltage would be selected to match the circuit being driven. In that case, there are no DC offsets to overcome so this application note will deal only with the most common implementations of LVPECL to LVPECL DC coupling.

LVPECL, PECL, ECL Logic and Termination

2.2 Termination when a Reference Voltage Exists

The simplest LVPECL termination scheme is depicted. However, this termination method requires a reference supply voltage at the input of the driven gate. The reference voltage is 2.0v below Vcc. This is added complication and expense which may not be appropriate for systems utilizing LVPECL in only selected signal paths.



2.3 Alternative 50 ohm termination - 3 Resistor Solution

An alternative method of terminating LVPECL which reduces the overhead to one additional resistor. The two 50 ohm resistors provide the needed signal termination, and the third resistor provides the path to ground to bias the termination resistors to V_{TT}.

For V_{CC} = 3.3V V_{HI} = 2.275V V_{LO} = 1.680V V_{TT} = 1.30V

For V_{CC} = 2.5V V_{HI} = 2.275V V_{LO} = 1.680V V_{TT} = 0.50V

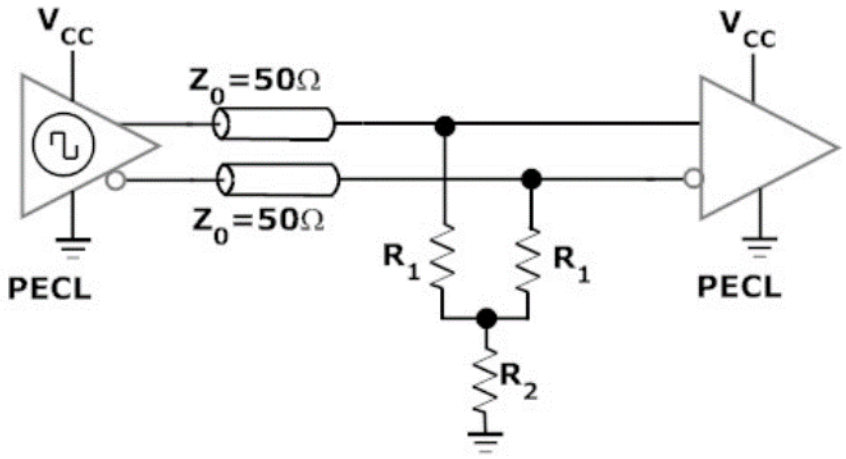
$$R2 = \frac{V_{TT}}{(V_{HI} + V_{LO}) * 0.5 - V_{TT}}$$

25

VCC	R1 (2 each)	R2
2.5V	50 ohms	16 ohms
3.3V	50 ohms	50 ohms

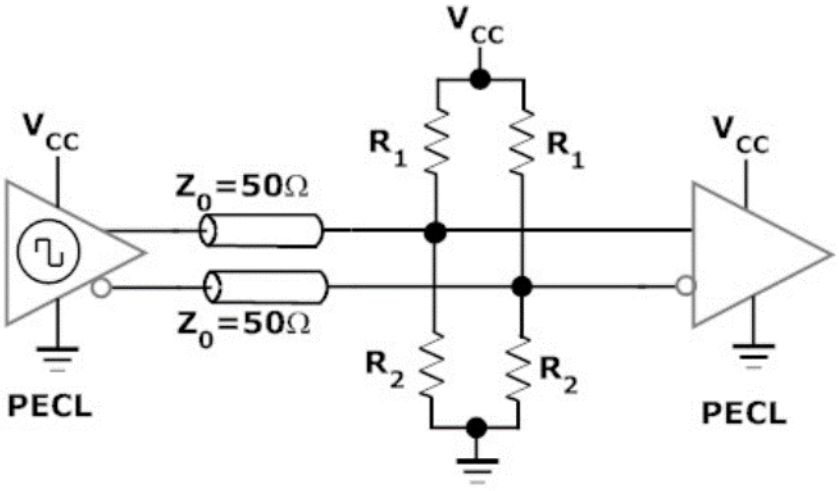
LVPECL, PECL, ECL Logic and Termination

Note: R2 calculates to be 48 ohms but simplified bill of materials, most use 50 ohms to make all three values the same.



2.4 Alternative 50 ohm termination - 4 Resistor Solution

This is probably the most common LVPECL termination method. The voltage dividers form a 50-Ohm therein equivalent termination, a DC paths for the emitter follower



LVPECL, PECL, ECL Logic and Termination

outputs and V_{TT} reference bias 2.0v below V_{CC} for the LVPECL inputs. Two added resistors is a small price to pay in order to eliminate the additional reference power supply. Note that the equations shown are for calculating terminating resistor values for 50Ω terminations only.

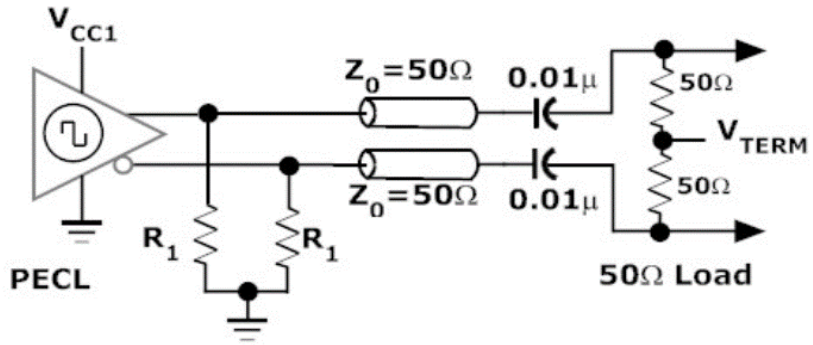
$$R1 \,//\, R2 = 50 \text{ ohms}$$

$$VCC \cdot \frac{R1}{R1 + R2} = 2.0V$$

VCC	R1 (2 each)	R2 (2 each)
2.5V	250 ohms	62.5 ohms
3.3V	130 ohms	83 ohms
5.0V	83 ohms	125 ohms

2.5 Single Resistor to Ground AC coupled 50 ohm termination

The PECL output can drive 50 ohm loads. This is an example of AC coupling to a 50 ohm load and the V_{TERM} value can be set to match the DC bias point of the load. R1 must be selected to bias the PECL emitter output.



Recommended resistor values:

V_{CC} = 3.3V R1 = 150 ohms

V_{CC} = 2.5V R1 = 95 ohms

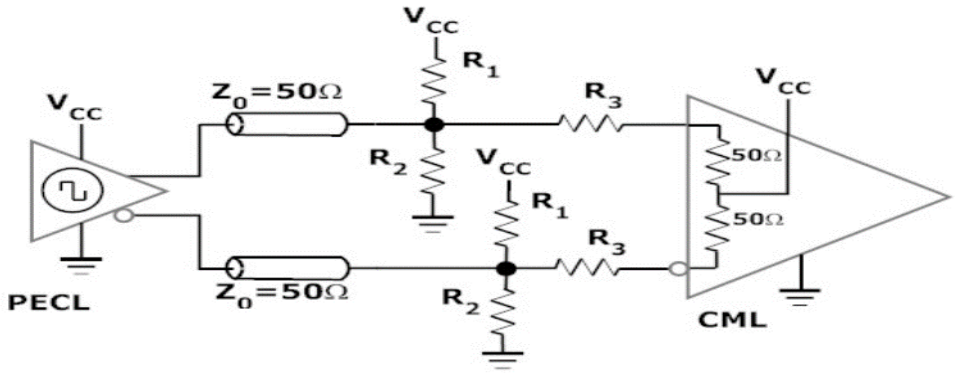
LVPECL, PECL, ECL Logic and Termination

3 Interfacing PECL Outputs to Other Logic Types

In addition to LVPECL to LVPECL connections, it is possible to use Pletronics LVPECL oscillators with other logic families. Among these are LVDS, CML and HSTL. Pletronics makes a complete line of LVDS oscillators, so adapting LVPECL to LVDS is not normally needed unless required at very high frequencies.

3.1 Interfacing PECL to CML

CML is similar to ECL and PECL. However, there are differences in voltage swing and termination networks. The differential voltage swing for CML is 400mv, versus 800mv for LVPECL. CML input structures include terminating resistors and may include a bias voltage source, thus eliminating the need for external components. The bias voltage used for CML is different from LVPECL so that is also a consideration.



The V_{CM} of the CML input and the signal swing on the CML input will need to use the minimum levels allowed. The CML input is reduced to about 0.125V PP which is still within the CML input minimum level specification. Therefore R3 is 275 ohms.

The values for R1 and R2 are chosen similar to Section 2.4. In this case, R1 is parallel with series combination of R3 and 50 ohm CML termination.

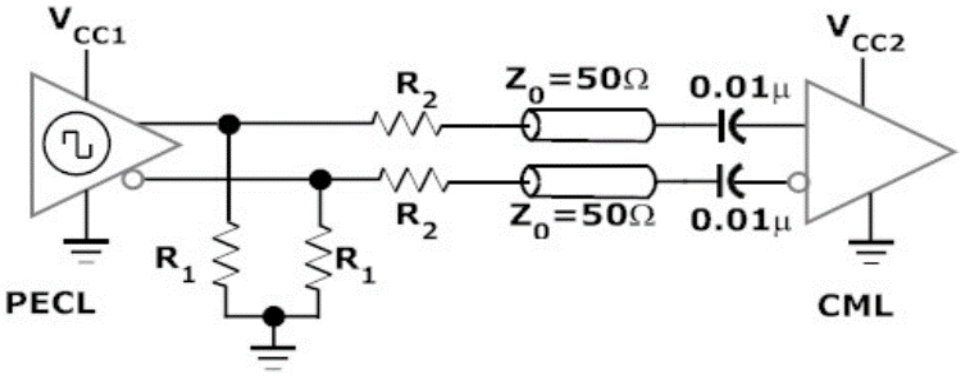
VCC	R1 (2 each)	R2 (2 each)	R3 (2 each)
2.5V	2,750 ohms	62.5 ohms	275 ohms
3.3V	208 ohms	83 ohms	275 ohms

LVPECL, PECL, ECL Logic and Termination

3.2 INTERFACING PECL TO CML WHEN INTERNALLY DC BIASED

The most widely used method for translating from LVPECL to CML is through AC-coupling. AC coupling removes any common mode voltage concerns between the LVDS oscillator and CML input stage. In some data applications, base line wander is a consideration in AC coupling schemes but this is not an issue with an oscillator. In this scheme, the two R1s provide a current return for the oscillator's emitter follower output stage. The two R2s reduce the LVPECL output voltage swing by approximately 40% for CML compatibility.

See Section 2.5 for a similar PECL output



VCC	R1 (2 each)	R2 (2 each)
2.5V	95 ohms	30 ohms
3.3V	150 ohms	30 ohms

3.3 INTERFACING PECL TO HSTL

The point 'a' on the schematic is the V_{TT} point (V_{CC} - 2.0V)for PECL terminations.

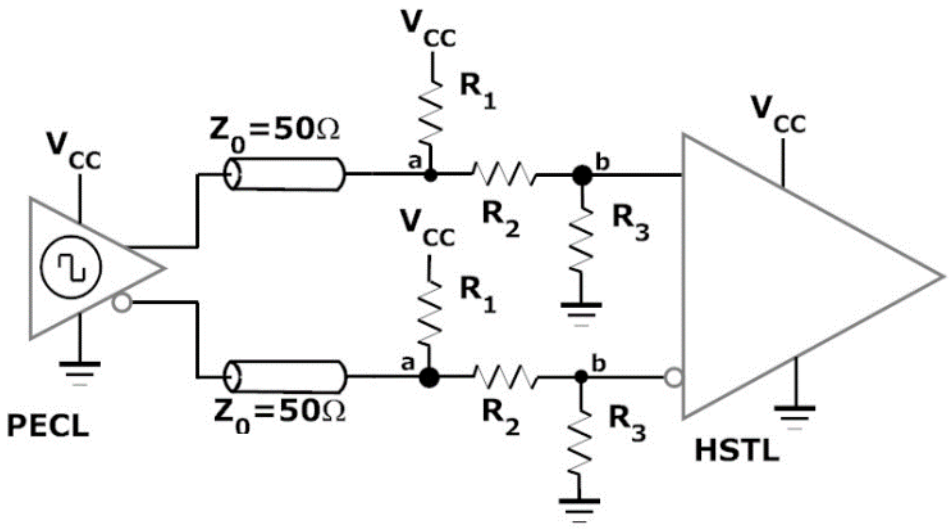
The point 'b' on the schematic is the V_{REF} of HSTL (0.75 V)

$$2.0\ V = VCC \frac{R1}{R1 + R2 + R3}$$

$$0.75\ V = VCC \frac{R3}{R1 + R2 + R3}$$

R1 // (R2 +R3) = 50 ohms (PECL termination)

LVPECL, PECL, ECL Logic and Termination



Unfortunately there are not "perfect" solutions for V_{CC} = 2.5V. There has to be a compromise in one of the parameters. There are two good.

V_{CC}	R1 (2 each)	R2 (2 each)	R3 (2 each)
2.5V[a]	100 ohms	40 ohms	60 ohms
2.5V[b]	118 ohms	25 ohms	62 ohms
3.3V	127 ohms	35 ohms	48 ohms

The 'a' solution results in a 50 ohm PECL termination and the HSTL V_{REF} being correct but the PECL termination is V_{TT} is only 1.25V. The HSTL signal will be 60% of the PECL signal.

The 'b' solution results in a 50 ohm PECL termination and the HSTL V_{REF} being correct but the PECL termination is V_{TT} is only 1.44V. The HSTL signal will be 71% of the PECL signal.

3.4 Interfacing PECL to LVDS attenuate PECL to LVDS Levels

The Pletronics LV9 family of LVDS outputs only operates to 700MHz. If higher frequency LVDS signals are needed, this PECL to LVDS interface provides solutions to the upper limit of the PE9 series.

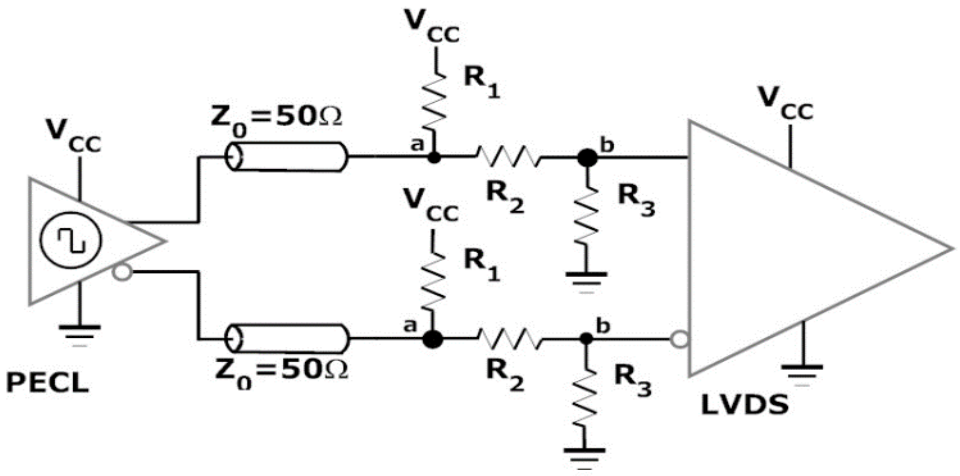
Some LVDS input cannot accept overdrive. This solution reduces the PECL peak-to-peak signal levels to LVDS levels, and level shifts the signal to the LVDS 1.2V input average level.

LVPECL, PECL, ECL Logic and Termination

$$V_{TT}\ (PECL) = 2.0\ V = VCC \frac{R1}{R1 + R2 + R3}$$

$$V_{REF}\ (LVDS) = 1.2\ V = VCC \frac{R3}{R1 + R2 + R3}$$

R1 // (R2 +R3) = 50 ohms (PECL termination)



There is not an exact solution for 3.3V. Here are optimum values to use: for 2.5V the schematic must change, move R1 from VCC to 'b' and move R3 from 'a' to ground.

VCC	R1 (2 each)	R2 (2 each)	R3 (2 each)
2.5V*	168 ohms	88 ohms	62.5 ohms
3.3V	107 ohms	21 ohms	73 ohms

NOTE: For 2.5V the schematic is changed!

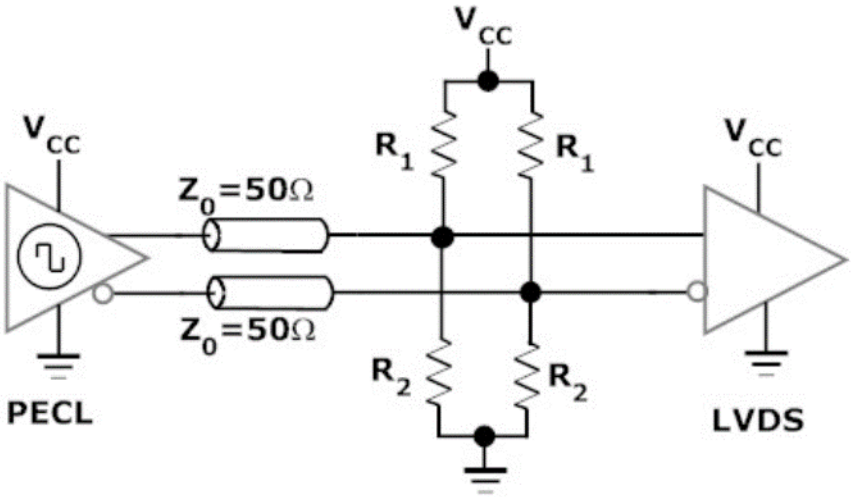
3.5 Interfacing PECL to LVDS when LVDS can Accept Larger Signal Levels

Many LVDS inputs will permit overdrive and have a wide common mode range. In this case the PECL level can be directly driven into the LVDS input. This results in a simpler

LVPECL, PECL, ECL Logic and Termination

circuit. The LVDS input specifications must be checked to determine if this condition is acceptable. This also assumes the LVDS terminations are external.

The terminations are standard PECL terminations.



VCC	R1 (2 each)	R2 (2 each)
2.5V	250 ohms	62.5 ohms
3.3V	130 ohms	83 ohms

4 Interfacing 3.3V PE9 Series to other PECL voltage devices

By and large, LVPECL at 3.3v (and more recently 2.5v) predominate over the older 5v PECL. For LVPECL applications, Pletronics offers the PE7 oscillator series in either 2.5v or 3.3v and the PE9 oscillator series in 3.3v. However, there are still applications which require 5v PECL oscillators. This is problematic since the manufacturing of 5v PECL oscillators is becoming obsolete.

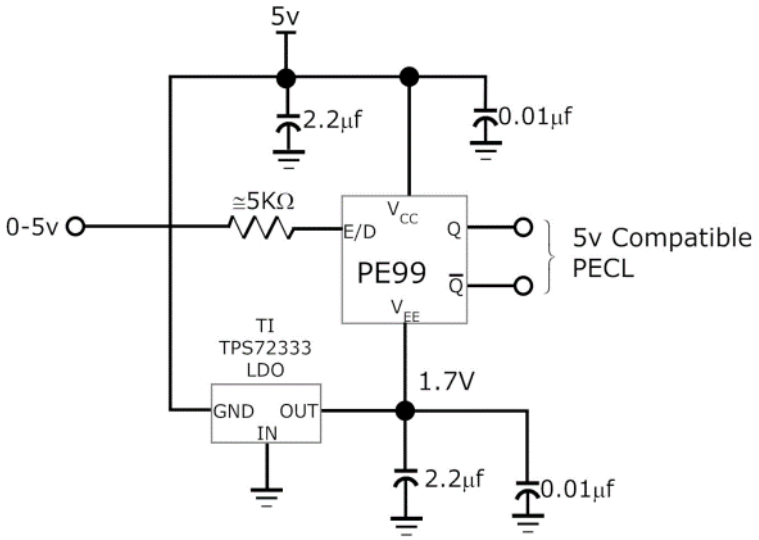
Additionally, the PE9 series are desired in 2.5V applications.

LVPECL, PECL, ECL Logic and Termination

4.1 Interfacing PE9 to 5.0V PECL

The first circuit, shown in Figure 6, is a method for connecting a Pletronics 3.3v LVPECL, PE99 oscillator to a 5v PECL load. The load circuit and terminating resistors are not shown but would be the same as for any 5v PECL connection. Even though the PE9 is shown, this method works equally well with the PE77 series XO or the VPU7 series VCXO. For the VCXO, additional consideration for the control input voltage range is required.

The Low Drop Output (LDO) regulator selected for this application is a negative voltage regulator. Any fixed or adjustable negative voltage regulator could be substituted. This regulator must sink current from the PE9 to ground.

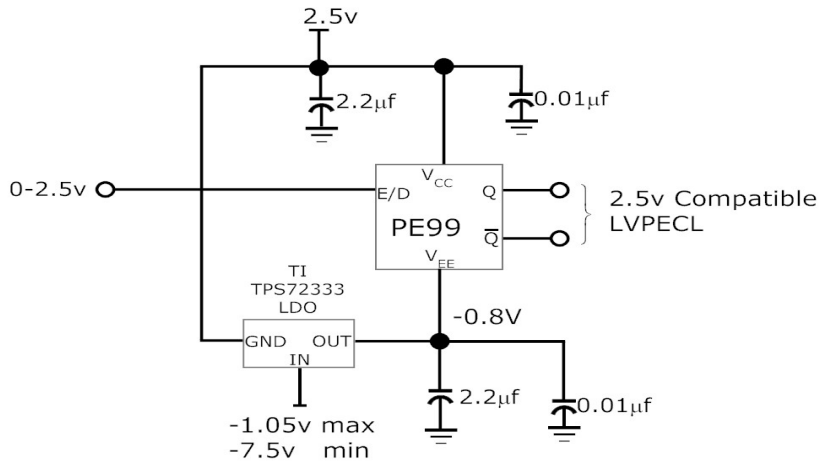


4.2 Interfacing PE9 to 2.5V PECL - DC Solution

In addition, the Pletronics PE9 and VPU7 VCXO series of 3.3v LVPECL oscillators offer great advantages in cost and performance in high frequency applications. Even though the PE9 and VPU7 are offered only in 3.3v they may be used in 2.5v LVPECL applications with only a bit of additional circuitry. For the price of a small LDO, there is potential for significantly increased performance and reduced cost.

LVPECL, PECL, ECL Logic and Termination

In the following circuit, a method is shown whereby a PE9 series oscillator may be used with a 2.5v LVPECL load. Merely using a 2.5v LVPECL oscillator like the PE77 series would seem to make this completely unnecessary. However, the PE9 and VPU7 series oscillators are designed using the latest SiGe processes and have significant performance, higher frequency and cost advantages over more traditional approaches using 3rd overtone crystals, SAW resonators, etc. Therefore, this approach may be preferred to many applications.



4.3 Interfacing PE9 to 2.5V PECL - AC Solution

An AC coupled resistive level shift can also be used to interface the PE9 series to 2.5V LVPECL solutions. At higher frequencies the layout of this approach is critical to keep the line lengths matched for the two output signals. The fact that the clock oscillator outputs are continuous stream of 50% duty cycle signals permits use of AC terminations. The noise immunity of this solution is compromised by the unmatched errors of the 3.3V and 2.5V supply. For optimum results the error should track.

R1	R2	R3	C1
50 ohms	18 ohms	52 ohms	0.01uF

The value of C1 will work well for clock frequencies 10MHz and above.